

MEASUREMENT OF TRANSISTOR HIGH-FREQUENCY CURRENT GAIN*

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Summary—An approach commonly used in instruments to test the high-frequency current gain of transistors consists of driving the base with a calibrated current source and measuring the collector current with a very low resistance meter. The major shortcomings of such instruments are their insufficient accuracy and their limited range of quiescent test conditions. However, a thorough analysis of this method demonstrates the possibility of reducing the measurement error, in the most unfavorable case, to less than 4.5 per cent as well as the possibility of extending the test conditions to $10\mu\text{V}$, $10\mu\text{A}$. These improvements were obtained as a result of the development of such features as a source impedance of $50\text{K}\Omega$ at 100Mc , a collector load of 1Ω and a very low capacitance socket.

I. INTRODUCTION

ONE OF THE USUAL circuits for measuring high-frequency grounded-emitter current gain is shown in the diagram of Fig. 1. The base current of the transistor-under-test (TUT) is supplied by a current source of adjustable amplitude and the collector current is sensed across a very low resistance R_L .

Measurements can be made by either of the following methods:

- 1) Constant input current or direct reading—with switch (s) in position (1), the current source is adjusted to give a unity voltage drop (for example, $1\mu\text{V}$) across R_L . Next, with the switch in position (2), the current i_1 is amplified by the TUT giving a new output current i_2 . The voltage reading across R_L is equal to the numerical value of $|h_{fe}|$.
- 2) Constant output current—with switch (s) in position (2), the input current is adjusted to a value i_1 for a given voltage reading across R_L . Next, with the switch in position (1), the current source is readjusted to a value i_1' for the same voltage reading across R_L . The ratio i_1'/i_1 is equal to the numerical value of $|h_{fe}|$.

The difficulty of creating the test conditions specified by the definition of $|h_{fe}|$ results in significant errors

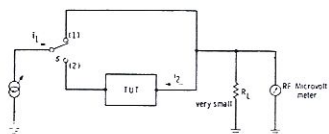


Fig. 1—Basic diagram of test circuit.

considered in Section III and evaluated in Section IV. In Section V, a detailed analysis of the relevant parameters

in $|h_{fe}|$ measurement reveals the critical elements of the test circuit.

II. DEFINITION OF h_{fe}

A transistor in common-emitter configuration can be represented by the following equations in which e_i , i_1 , e_o , i_2 are the small-signal input and output voltages and currents:

$$e_i = h_{ie}i_1 + h_{re}e_o, \quad (1)$$

$$i_2 = h_{fe}i_1 + h_{oe}e_o. \quad (2)$$

By definition, h_{fe} is the small-signal common-emitter forward-transfer current ratio with the output shorted. The absolute value of this parameter¹, given by (3), can be measured by the method described herein.

$$|h_{fe}| = \left| \frac{i_2}{i_1} \right|. \quad (3)$$

III. EXPERIMENTAL DIFFICULTIES AND LIMITATIONS

As shown in Fig. 2, a true measurement of $|h_{fe}|$ requires:

- 1) An ideal current source.
- 2) An ideal current meter of zero-input impedance with sufficient sensitivity to detect infinitesimal currents.

Although these requirements cannot be fulfilled in practice, it is possible to simulate nearly perfect conditions by treating the input current source and the output current meter as described in Sections A and B below.

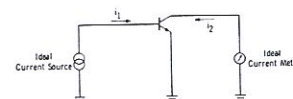


Fig. 2—Ideal test circuit.

A. Input Current Source

The usual method of obtaining a current source is to place a large impedance Z_s in series with a voltage generator as shown in Fig. 3 where Z_{ie} represents the input of the TUT.

¹ It has been customary to refer to the magnitude of the high-frequency current gain as h_{fe} . It should not be overlooked, however, that this symbol represents a complex number.

A simple resistor R_s could be used for Z_s , but at the frequencies considered, the shunt capacitance across R_s limits the equivalent source impedance. For example, at 100Mc, a 1-pf capacitance has a reactance of only 1.6K Ω . A considerable improvement can be made in reducing the shunt capacitance by using a few resistors in series for Z_s . Best results are obtained when a very small capacitor C_s is substituted for the resistor. A suitable value for C_s is 0.03 pf which has a reactance of 50 K Ω at 100 Mc.

Let

- C_s = series capacitance of the source
- C'_{be} = capacitance from the base contact of the socket to ground (wiring strays and base tuning trimmer included)
- C'_{ce} = capacitance from the collector contact of the socket to ground (wiring strays included)
- C'_{cb} = capacitance from the collector contacts to the base contact of the socket
- R_L = collector load ($< 10 \Omega$).

Some of the current supplied through C_s is lost in the circuit and socket capacitances shown in Fig. 4, thereby reducing the equivalent source impedance.

The capacitance C'_{ce} is smaller than 1pf and represents a reactance greater than 1.6 K Ω at 100 Mc; if R_L is less than 10 Ω , C'_{ce} can be neglected.

The capacitance from the base terminal of the socket to ground C'_{be} can be neutralized by an inductor L'_{be} of sufficiently high Q for the loss current in the tank circuit $C'_{be} L'_{be}$ to be negligible compared to the base current of the TUT.

Neutralization of the collector-to-base socket capacitance C'_{cb} with an inductor L'_{cb} could be attempted. The geometry of the system, however, would imply a close proximity of inductors L'_{cb} and L'_{be} resulting in a certain amount of undesirable coupling between the two coils. Instead of using this second inductor, which among other difficulties would involve a very complicated tuning procedure, special low-capacitance sockets have been designed which give satisfactory results.

The above considerations are shown schematically in Fig. 5.

B. Output Current Measurement

According to the definition of $|h_{fe}|$ the ac output should be very small—for instance, less than one tenth of the quiescent current. Since it is sometimes necessary to measure $|h_{fe}|$ at collector currents as low as 50 μ a dc, the ac signal should be limited to a few microamperes. Furthermore, to satisfy the shorted output condition specified in Section II, the value of R_L should be negligible compared to h_{oe}^{-1} , for example, R_L less than 10 Ω .

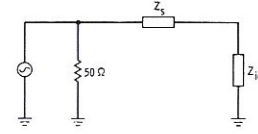


Fig. 3—High impedance source.

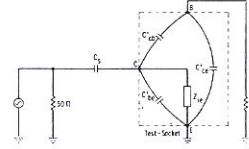


Fig. 4—Test circuit showing wiring and socket stray capacitances.

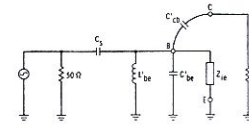


Fig. 5—Simplified test circuit.

IV. EVALUATION OF THE MEASUREMENT ERRORS

Consider the equivalent diagram of the test circuit, shown in Fig. 6, which is based upon the remarks of Section III.

The source admittance Y_s is the Thevenin equivalent resulting from C_s and the conductance g'_{be} of the tank circuit $C'_{be} L'_{be}$. The TUT is represented in the common-emitter configuration, and Y_a is the admittance of the capacitance C'_{cb} . Y_L is the load admittance. The Y parameters of the transistor shunted by Y_a are as follows:

$$\begin{aligned} Y_{11} &= Y_i + Y_a \\ Y_{12} &= Y_r - Y_a \\ Y_{21} &= Y_f - Y_a \\ Y_{22} &= Y_o + Y_a \end{aligned} \quad (4)$$

In Fig. 6, the current i_2 is given by the following (see derivation in Appendix A):

$$i_2 = I h_{fe} [1 - (\gamma + \delta + \eta) + \gamma(\epsilon + \delta + \eta) + \delta\eta] \quad (5)$$

where

$$\gamma = \frac{Y_s}{Y_i} \quad (6)$$

$$\delta = \frac{Y_a}{Y_i} \left(1 + \frac{1}{h_{fe}} \right) \quad (7)$$

$$\epsilon = \frac{Y_a}{Y_i} + h_{fe} \frac{Y_a - Y_r}{Y_L} \quad (8)$$

$$\eta = \frac{1}{Y_L} [Y_a + Y_o + h_{fe}(Y_a - Y_r)] \quad (9)$$

The above parameters satisfy the following inequalities justified in Section VI:

$$|\gamma| \ll 1 \quad (10)$$

$$|\delta| \ll 1 \quad (11)$$

$$|\epsilon| \ll 1 \quad (12)$$

$$|\eta| \ll 1. \quad (13)$$

For the purpose of this analysis, the inequality $\ll 1$ will be considered satisfied when the condition < 0.1 holds.

Neglecting the second-order terms, (5) becomes

$$i_2 = Ih_{fe}[1 - (\gamma + \delta + \eta)]. \quad (14)$$

To determine the value of $|h_{fe}|$, (14) is analyzed to two successive approximations which are discussed next.

1) *First Approximation*: If the quadrupole Y in Fig. 6 is replaced with a short circuit as shown in Fig. 7, the voltage reading across Y_L corresponds to $|h_{fe}| = 1$. This can be performed by plugging into the test socket a transistor header with a base-to-collector short.

The resulting output current i'_2 is given by

$$i'_2 = -I \frac{Y_L}{Y_s + Y_L} = -I \frac{1}{1 + Y_s/Y_L} \quad (15)$$

and since the condition $Y_s/Y_L < 10^{-3}$ is easily satisfied, it reduces to

$$i'_2 \simeq -I. \quad (16)$$

When the transistor to be tested is plugged into the socket, the output current i_2 flowing through Y_L is given by (14). Eq. (14) divided by (16) yields

$$\frac{i_2}{i'_2} = -h_{fe} [1 - (\gamma + \delta + \eta)] \quad (17)$$

$$h_{fe} = -\frac{i_2}{i'_2} [1 + (\gamma + \delta + \eta)].$$

If $(-i'_2)$ is adjusted to a unity value, the current gain becomes

$$h_{fe} = i_2 + (\gamma + \delta + \eta)i_2. \quad (18)$$

All the symbols in the foregoing relations are complex quantities. The factor $(\gamma + \delta + \eta)$ which is indeterminate for an unknown TUT will be considered to represent the error σ_1 of the first approximation. The absolute value of h_{fe} is therefore

$$|h_{fe}| = |i_2| \pm S |(\gamma + \delta + \eta)i_2| \\ = |i_2| \pm S\sigma_1 |i_2| \quad (19)$$

where S is a positive real number equal to or less than one.

2) *Second Approximation*: Assuming for this particular purpose that the circuit of Fig. 8 is a suitable representation of the input of the TUT, Y_i can be determined by using the value of $|h_{fe}|$ obtained in the first approximation.

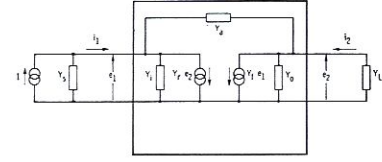


Fig. 6—Equivalent diagram of the test circuit.

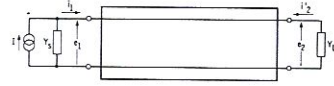


Fig. 7—Quadrupole Y replaced with a short circuit.

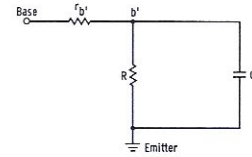


Fig. 8—Input model of TUT.

Let

$r_{b'}$ = base spreading resistance

$$R = (h_{FE} + 1)r_e \quad (20)$$

$$r_e = \frac{26(\text{mv})}{I_c(\text{ma})} \quad (21)$$

$$C = \frac{1}{R\omega_0} = \frac{h_{FE}}{(1 + h_{FE})r_e\omega_T} \simeq \frac{1}{r_e\omega_0} = \frac{1}{r_e\omega_0 |h_{fe}|} \quad (22)$$

where

ω_0 = operating radian frequency

h_{FE} = low-frequency small-signal short-circuit current gain

ω_T = short-circuit current-gain radian-frequency product.

The admittance of the RC network is

$$Y_{b'e} = \frac{1}{R} + j\omega_0 C = \frac{1}{(h_{FE} + 1)r_e} + j \frac{1}{|h_{fe}| r_e} \\ \simeq \frac{1}{r_e} \left(\frac{1}{h_{FE}} + j \frac{1}{|h_{fe}|} \right). \quad (23)$$

Therefore, the input admittance of the TUT has the approximate value

$$Y_i \simeq \frac{\frac{1}{r_{b'}} + \frac{1}{r_e} \left(\frac{1}{h_{FE}} + j \frac{1}{|h_{fe}|} \right)}{\frac{1}{r_{b'}} + \frac{1}{r_e} \left(\frac{1}{h_{FE}} + j \frac{1}{|h_{fe}|} \right)} \\ = \frac{1}{r_{b'} + \frac{r_e}{\frac{1}{h_{FE}} + j \frac{1}{|h_{fe}|}}} \quad (24)$$

Given Y_s and Y_a , it is possible to evaluate the parameter $\gamma = Y_s/Y_i$ and also the parameter² $\delta \simeq Y_a/Y_i$ if $|h_{fe}| > 5$. Accordingly, the sum $\gamma + \delta$ becomes

$$\gamma + \delta = \frac{Y_s}{Y_i} + \frac{Y_a}{Y_i} = \frac{Y_s + Y_a}{Y_i} = (Y_s + Y_a) \left[r_{be} + \frac{r_e}{\frac{1}{h_{FE}} + j \frac{1}{|h_{fe}|}} \right] \quad (25)$$

To obtain the second approximation instead of a shorted header, an admittance Y'_i is inserted between the base and collector terminals of the socket. This admittance should be such that the error term $(\gamma + \delta)$ in (5) is cancelled. The new configuration is shown in Fig. 9.

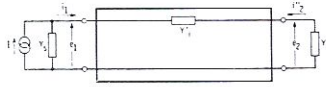


Fig. 9—Quadrupole Y replaced with Y'_i .

Neglecting Y_L , and given³ that $Y_s/Y_i \ll 1$, the resulting output current i_2'' has the value

$$i_2'' \simeq -I \frac{Y'_i}{Y_s + Y'_i} = I \frac{1}{1 + Y_s/Y'_i} \simeq -I \left(1 - \frac{Y_s}{Y'_i} \right) \quad (26)$$

Making Y'_i equal to

$$Y'_i = \frac{Y_s Y_i}{Y_s + Y_a} \quad (27)$$

and substituting (27) in (26), i_2'' becomes

$$i_2'' = -I \left(1 - \frac{Y_s}{Y'_i} \right) = I \left(1 - \frac{Y_s + Y_a}{Y_i} \right) = -I[1 - (\gamma + \delta)] \quad (28)$$

Dividing (14) by (28) results in

$$\frac{i_2}{i_2''} = -h_{fe} \left[1 - \frac{\eta}{1 - (\gamma + \delta)} \right] \simeq -h_{fe} [1 - \eta] \quad (29)$$

The error terms γ and δ have now been cancelled and the small-signal current gain is

$$h_{fe} = -\frac{i_2}{i_2''} (1 + \eta) \quad (30)$$

² When this condition is not satisfied an estimate of the phase of h_{fe} can be made and the relation

$$\delta = \frac{Y_a}{Y_i} \left(1 + \frac{1}{h_{fe}} \right)$$

must be used instead of $\delta = Y_a/Y_i$.

³ Refer to Tables I, II and III.

Adjusting $(-i_2')$ to unity value (30) becomes

$$h_{fe} = i_2 + \eta i_2 \quad (31)$$

The factor η will be considered to represent the error σ_2 of the second approximation. Therefore,

$$|h_{fe}| = |i_2| \pm S | \eta i_2 | = |i_2| \pm S \sigma_2 |i_2| \quad (32)$$

where S is a real number equal to or less than one.

To summarize the results of this analysis, the errors σ_1 and σ_2 obtained with the first and second approximations are given below as functions of the parameters defined by (6)–(9).

$$\sigma_1 \simeq |\gamma + \delta + \eta| \times 100 \text{ per cent} \quad (33)$$

$$\sigma_2 \simeq |\eta| \times 100 \text{ per cent} \quad (34)$$

V. DISCUSSION OF THE RELEVANT PARAMETERS IN $|h_{fe}|$ MEASUREMENT

A. Source Admittance Y_s

Fig. 10 shows the input current source circuit. The capacitance C'_e which includes strays and a trimmer is made as small as possible to minimize the loss conductance g'_{be} . The inductor L'_{be} is shielded to minimize any inductive coupling with the rest of the circuit. The series capacitor C_s is a fraction of a picofarad representing a very high reactance at the operating frequency. It can be made of a plastic rod with a longitudinal hole where two wires can slide, providing adjustment of the capacitance between them.

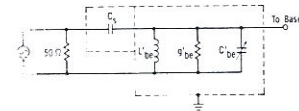


Fig. 10—Input current source circuit.

Considering the generator loaded with 50Ω as a voltage source, and assuming that L'_{be} is exactly tuned with C'_e , Y_s is given by

$$Y_s = g'_{be} + j\omega C_s \quad (35)$$

The capacitor C_s can be adjusted to approximately 0.03 pf. The values obtained for g'_{be} at 20 Mc and 100 Mc, as well as ωC_s and $|Y_s|$ at the same frequencies, are given in Table I.

TABLE I

f	g'_{be}	ωC_s	$ Y_s $
20 Mc	4 μmho	4 μmho	5.6 μmho
100 Mc	10 μmho	20 μmho	22 μmho

B. Collector-to-Base Socket Admittance Y_a

The stray capacitance between the collector and base contacts of the socket is a major cause of error. The available sockets on the market have strays between adjacent pins in the order of 1 pf which represents 0.62 millimho at 100 Mc, and, as mentioned in Section III, neutralization of this capacitance is not advisable. To minimize Y_a , special sockets with less than 0.1 pf between adjacent pins have been designed. They are described in detail in Appendix B.

The admittance Y_a is given by

$$Y_a = j\omega C'_{cb}. \quad (36)$$

Table II shows the values of $|Y_a|$ at 20 and 100 Mc for C'_{cb} equal to 0.1 pf.

TABLE II

f	$ Y_a $
20 Mc	12.5 μ mho
100 Mc	62.5 μ mho

C. Load Admittance Y_L

The collector of the TUT is connected to a load resistance in series with a decoupling capacitor as shown in Fig. 11. If the decoupling capacitor is made series resonant at the operating frequency with the lead inductance from the collector pin of the socket to ground, the load will be purely resistive and equal to R_L (10 ohms or less).

To obtain satisfactory results with the second approximation the error term should be made very small. This can be achieved with the scheme of Fig. 12 in which the collector decoupling capacitor is carefully chosen so that the reactance from the socket clip to ground is zero at the operating frequency. The transformer is made of a ferrite core and has one turn in the primary and five turns in the secondary. The resultant load admittance Y_L is then equal to 1000 millimhos.

D. Input Admittance of the Transistor Y_i

At high frequencies an approximate value of the input admittance can be derived from the hybrid- π equivalent (Fig. 13). The minimum of Y_i occurs at very low currents in which case the admittance $[1/(h_{FE} + 1)r_e + j\omega C_{b'e}]$ is negligible compared to $j\omega(C_{Te} + C_c)$. Also, r_b' can be neglected because it is in series with a much higher reactance $1/j\omega(C_{Te} + C_c)$. Therefore, a satisfactory approximation of the minimum input admittance is given by the parallel combination of

$$(C_{Te} + C_c + C_{b'e}) = (C_{Te} + C_{ob}) \quad \text{and} \quad 1/r_b'c: \quad (37)$$

$$Y_i = g_i + jb_i = 1/r_b'c + j\omega(C_{Te} + C_{ob}).$$

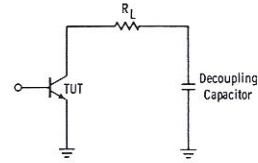


Fig. 11—Load of the TUT.

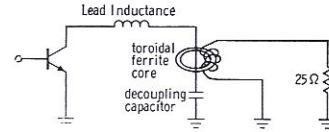


Fig. 12—Transformer coupled output circuit.

TABLE III

f	b_i
20 Mc	0.25 millimho
100 Mc	1.25 millimho

For the fastest transistors available at present, $C_{Te} + C_{ob}$ is approximately 2 pf. Table III gives the values of b_i for $(C_{Te} + C_{ob})$ equal to 2 pf at 20 Mc and 100 Mc.

E. Output Admittance Y_o

At very low currents, the minimum of $|Y_o|$ can be approximated by (see Fig. 13)

$$|Y_o| = |g_o + jb_o| \simeq \omega C_{ob} \quad (38)$$

where ω is the operating radian frequency and

$$C_{ob} = C_c + C_{b'e}.$$

A reasonable value for the minimum of C_{ob} is 1 pf which establishes the minimum of b_o . On the other hand, the maximum of $|Y_o|$ is determined by the following assumption:

$$|h_{fe}| \cdot |Y_o| < 20 \text{ millimho}. \quad (39)$$

Eq. (39) states simply that it is not of general interest to make measurements at high frequencies (above 20 Mc) with transistors of very large output admittance. The maximum of $|h_{fe}| \cdot |Y_o|$ is thus considered equal to 20 millimhos.

Table IV gives the values of b_o for C_{ob} equal to 1 pf at 20 Mc and 100 Mc.

F. Reverse-Transfer Admittance Y_r

The reverse-transfer admittance is generally independent of the collector current. Its real part g_r varies only slightly and its imaginary part b_r decreases with increasing collector-to-emitter voltage.

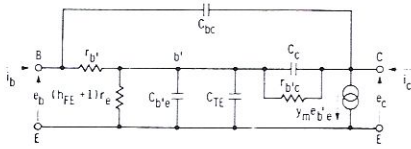


Fig. 13—Hybrid-pi model of the transistor.

TABLE IV

f	b_0
20 Mc	125 μmho
100 Mc	625 μmho

The following inequality between Y_r and Y_o is generally satisfied.

$$|Y_r| < |Y_o|. \quad (40)$$

Also, g_r and b_r are opposite in sign to g_o and b_o .

VI. JUSTIFICATION OF THE ASSUMPTIONS OF SECTION IV

The considerations of Section V lead to the simple justification of inequalities (10)–(13) as follows:

A. Inequality (10)

From (6)

$$|\gamma| = \left| \frac{Y_s}{Y_i} \right| = \left| \frac{Y_s}{Y_i} \right| < \left| \frac{Y_s}{b_i} \right|. \quad (41)$$

$|Y_s|$ being fixed for a given operating frequency, the maximum of $|\gamma|$ corresponds to the minimum of b_i . The values of Tables I and III show that

$$|\gamma| \leq 0.022 \quad \text{at} \quad 20 \text{ Mc} \quad (42)$$

$$|\gamma| \leq 0.018 \quad \text{at} \quad 100 \text{ Mc} \quad (43)$$

which proves (10).

B. Inequality (11)

From (7)

$$|\delta| = \left| \frac{Y_a}{Y_i} \left(1 + \frac{1}{h_{fe}} \right) \right| = \left| \frac{Y_a}{Y_i} \right| \left| 1 + \frac{1}{h_{fe}} \right| < \left| \frac{Y_a}{b_i} \right| \left| 1 + \frac{1}{h_{fe}} \right|. \quad (44)$$

As shown in Section V-D, the minimum of b_i occurs at very low currents. Besides, it can be assumed that the test is made at a frequency below f_r in which case $|h_{fe}|$ is at least equal to one and $|1 + 1/h_{fe}|$ is less than two. For the most unfavorable situation, a comparison between the values of Tables II and III at both 20 and 100 Mc shows that

$$\delta < 0.05 \times 2 = 0.1.$$

If the phase of h_{fe} is taken into consideration it can be shown that $|1 + 1/h_{fe}|$ is close to, but less than one. In

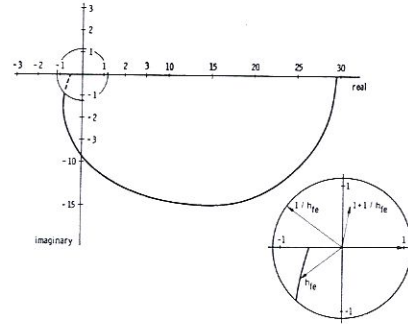


Fig. 14—Typical complex plot of h_{fe} .

fact, at low frequencies, $|h_{fe}|$ is large and $|1/h_{fe}| \ll 1$, and at high frequencies, $|1/h_{fe}|$ is close to one but its phase (including the excess phase) is normally larger than $2\pi/3$ (see Fig. 14).

Inequality (11) is, therefore, completely justified.

C. Inequality (12)

From (8)

$$|\epsilon| = \left| \frac{Y_a}{Y_i} + h_{fe} \frac{Y_a - Y_r}{Y_L} \right| < \left| \frac{Y_a}{b_i} \right| + |h_{fe}| \left| \frac{Y_a - Y_r}{Y_L} \right|. \quad (45)$$

According to relation (40) and taking into consideration the opposite sign of the real and imaginary parts of Y_r and Y_o , the expression $|Y_a - Y_r|$ can be replaced in the above inequality by the greater quantity $|Y_a + Y_o|$.

The values of Table II and IV show that $|Y_a| < 0.1b_0 < 0.1|Y_o|$ so that (45) can be replaced by

$$|\epsilon| < \left| \frac{Y_a}{b_i} \right| + 1.1 \left| \frac{h_{fe}}{Y_L} \right| |Y_o|. \quad (46)$$

Replacing in this expression Y_L by 1000 millimhos, $|Y_a|/b_i$ by 0.05 (see Tables II and III) and taking into consideration (39), it follows that

$$|\epsilon| < 0.072 \quad (47)$$

which proves (12).

D. Inequality (13)

From (9)

$$|\eta| = \left| \frac{1}{Y_L} \right| \cdot |Y_a + Y_o + h_{fe}(Y_a - Y_r)|. \quad (48)$$

The considerations made upon $|\epsilon|$ apply as well for $|\eta|$,

$$\begin{aligned} |\eta| &< \left| \frac{1}{Y_L} \right| \cdot |h_{fe} + 1| \cdot |Y_a + Y_o| \\ &< 1.1 \left| \frac{1}{Y_L} \right| \cdot |h_{fe} + 1| \cdot |Y_o| \\ &< 2.2 \left| \frac{h_{fe}}{Y_L} \right| |Y_o| \end{aligned} \quad (49)$$

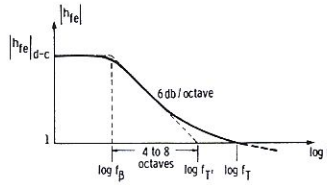


Fig. 15—Variation of $|h_{fe}|$ as a function of frequency.

giving

$$|\eta| < 0.044 \quad (50)$$

which proves (13).

VII. CONCLUSION

A typical plot of $|h_{fe}|$ as a function of frequency is shown in Fig. 15. Two measurements, one at low frequency and the other in the 6 db/octave region, completely determine the significant part of this plot.

In the vicinity of and above f_T , the curve $|h_{fe}|/f$ does not follow a 6 db/octave slope; furthermore, the error term $\delta = Y_a/Y_i(1 + 1/h_{fe})$ becomes very large. Measurements in this region should therefore be avoided.

Accuracy depends largely upon the quiescent conditions of the TUT. The first line of Table V shows the values of the terms $|\gamma|$, $|\delta|$, $|\eta|$, as well as the worst case errors σ_1 and σ_2 obtained with the first and second approximations.

TABLE V*

	$ \gamma $	$ \delta $	$ \eta $	σ_1	σ_2
Worst Case	<2 per cent	<10 per cent	<4.4 per cent	<16.4 per cent	<4.4 per cent
Typical Case	<0.5 per cent	<1.5 per cent	<1.5 per cent	<3 per cent	<1.5 per cent

* These values do not include the reading error and the meter accuracy.

The second line shows the same parameters for a typical case such as the Fairchild Transistor 2N918 with the following quiescent conditions:

$$1 \text{ ma} < I_c < 50 \text{ ma}$$

$$1 \text{ v} < V_{CE} < 15 \text{ v.}$$

According to Table V, the first approximation is satisfactory in most cases where the test conditions do not require a very low dc current. When measuring at very low dc currents, however, the procedure of the second approximation ought to be followed.

In the test of transistor lots having similar characteristics the general method of the second approximation can be applied with the value of Y_i' determined with a typical Y_i .

APPENDIX

A. Derivation of the relation (5) giving the output current i_2 as a function of h_{fe}

The input current i_1 is given by (see Fig. 6)

$$i_1 = I \frac{Y_{in}}{Y_s + Y_{in}} = I \frac{1}{1 + Y_s/Y_{in}} \quad (51)$$

where the input admittance Y_{in} has the value

$$Y_{in} = Y_{11} - \frac{Y_{12}Y_{21}}{Y_{22} + Y_L} \quad (52)$$

By means of (52), the ratio Y_s/Y_{in} can be expressed as follows:

$$\frac{Y_s}{Y_{in}} = \frac{Y_s}{Y_{11} - \frac{Y_{12}Y_{21}}{Y_{22} + Y_L}} \quad (53)$$

Substituting (4), this ratio becomes

$$\begin{aligned} \frac{Y_s}{Y_{in}} &= \frac{Y_s}{Y_i + Y_a - \frac{(Y_r - Y_a)(Y_f - Y_a)}{Y_o + Y_a + Y_L}} \\ &= \frac{Y_s}{Y_i} \cdot \frac{1}{1 + \frac{Y_a}{Y_i} - \left(h_{fe} - \frac{Y_a}{Y_i}\right) \frac{Y_r - Y_a}{Y_o + Y_a + Y_L}} \end{aligned} \quad (54)$$

The expression $(Y_o + Y_a)$, given by the values of Tables II and IV, is negligible compared with Y_L which is equal to 1000 millimhos. Also, the ratio Y_a/Y_i is less than 0.05 and can be neglected when compared with h_{fe} , which is assumed to be equal to or greater than one (see Tables II and III).

It follows that

$$\frac{Y_s}{Y_{in}} \approx \frac{Y_s}{Y_i} \cdot \frac{1}{1 + \frac{Y_a}{Y_i} + h_{fe} \frac{Y_r - Y_a}{Y_L}} \quad (55)$$

Substituting the parameters defined in (6) and (8), it becomes

$$\frac{Y_s}{Y_{in}} \approx \gamma \frac{1}{1 + \epsilon} \quad (56)$$

According to assumptions (10) and (12) the above ratio can be written as

$$\frac{Y_s}{Y_{in}} \approx \gamma(1 - \epsilon) \quad (57)$$

which shows that this ratio also satisfies the inequality

$$\frac{Y_s}{Y_{in}} \ll 1. \quad (58)$$

Substituting (57) into (51) and taking into account (58), i_1 becomes

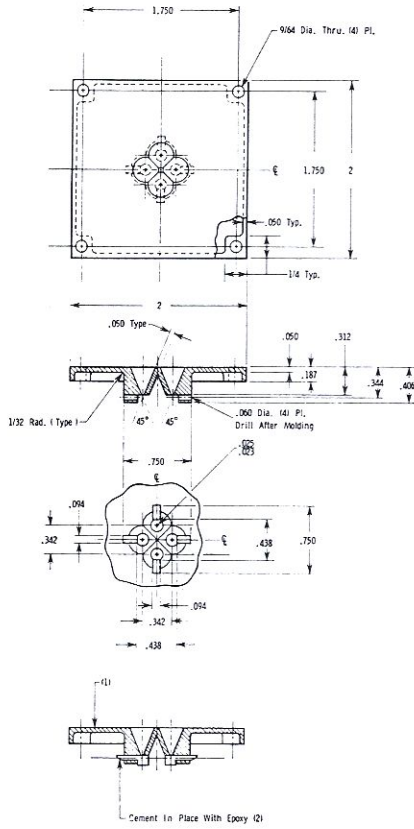


Fig. 16—Diagram of test socket for TO-5, TO-18, transistor cans and similar configurations.

$$i_1 = I \frac{1}{1 + \gamma(1 - \epsilon)} \approx I[1 - \gamma(1 - \epsilon)]. \quad (59)$$

Next, consider the ratio (see Fig. 6)

$$\frac{i_2}{i_1} = \frac{Y_{21}}{Y_{11} + \Delta/Y_L} = \frac{Y_{21}}{Y_{11}} \cdot \frac{1}{1 + \Delta/Y_{11}Y_L} \quad (60)$$

where Δ is the determinant ($Y_{11}Y_{22} - Y_{12}Y_{21}$).

Substituting (4), Y_{21}/Y_{11} can be expressed as follows:

$$\begin{aligned} \frac{Y_{21}}{Y_{11}} &= \frac{Y_f - Y_a}{Y_i + Y_a} = \frac{Y_f}{Y_i} \cdot \frac{1 - Y_a/Y_f}{1 + Y_a/Y_i} \\ &= h_{fe} \frac{1 - Y_a/Y_f}{1 + Y_a/Y_i} \end{aligned} \quad (61)$$

But $Y_a/Y_i \ll 1$, consequently

$$\begin{aligned} \frac{Y_{21}}{Y_{11}} &\approx h_{fe} \left(1 - \frac{Y_a}{Y_f}\right) \cdot \left(1 - \frac{Y_a}{Y_i}\right) \\ &= h_{fe} \left[1 - \left(\frac{Y_a}{Y_f} + \frac{Y_a}{Y_i}\right) + \frac{Y_a^2}{Y_f Y_i}\right]. \end{aligned} \quad (62)$$

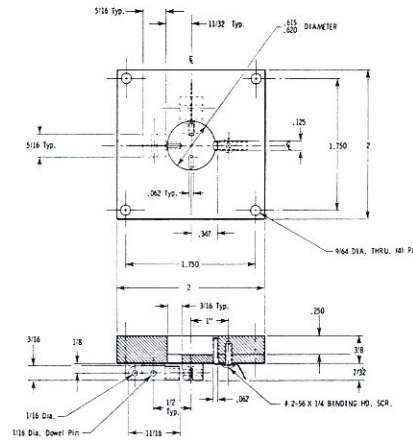


Fig. 17—Diagram of test socket for stud mount power package.

Also, $Y_f > Y_i$; therefore, $Y_a^2/Y_f Y_i$ is negligible compared to the other terms inside the bracket in (62). It follows that

$$\frac{Y_{21}}{Y_{11}} \approx h_{fe} \left[1 - \frac{Y_a}{Y_i} \left(1 + \frac{1}{h_{fe}}\right)\right]. \quad (63)$$

Substituting the parameter δ defined in (7), (63) becomes

$$\frac{Y_{21}}{Y_{11}} \approx h_{fe}(1 - \delta). \quad (64)$$

On the other hand, $\Delta/Y_{11}Y_L$ in (60) can be modified as follows:

$$\frac{\Delta}{Y_{11}Y_L} = \frac{Y_{11}Y_{22}}{Y_{11}Y_L} - \frac{Y_{12}Y_{21}}{Y_{11}Y_L} = \frac{1}{Y_L} \left(Y_{22} - \frac{Y_{12}Y_{21}}{Y_{11}}\right). \quad (65)$$

Substituting (4), (65) yields

$$\begin{aligned} \frac{\Delta}{Y_{11}Y_L} &= \frac{1}{Y_L} \left[Y_0 + Y_a - \frac{(Y_f - Y_a)(Y_f - Y_a)}{Y_i + Y_a}\right] \\ &= \frac{1}{Y_L} \left[Y_0 + Y_a + \frac{Y_f}{Y_i} \cdot (Y_a - Y_f) \cdot \frac{1 - Y_a/Y_f}{1 + Y_a/Y_i}\right]. \end{aligned} \quad (66)$$

But $Y_a/Y_i \ll 1$ and $Y_f > Y_i$, therefore $Y_a/Y_f \ll 1$. Consequently,

$$\frac{1 - Y_a/Y_f}{1 + Y_a/Y_i} \approx 1. \quad (67)$$

Substituting η defined in (9), (66) reduces to

$$\frac{\Delta}{Y_{11}Y_L} \approx \eta. \quad (68)$$

Using (64) and (68), i_2/i_1 given by (60) can be written

$$\frac{i_2}{i_1} = h_{fe}(1 - \delta) \frac{1}{1 + \eta}. \quad (69)$$

Taking into account assumption (13), the current i_2 becomes

$$i_2 \simeq i_1 h_{fe} (1 - \delta)(1 - \eta). \quad (70)$$

Replacing i_1 with (59) gives the result

$$i_2 = I h_{fe} [1 - \gamma(1 - \epsilon)](1 - \delta)(1 - \eta) \quad (71)$$

or

$$i_2 = I h_{fe} [1 - (\gamma + \delta + \eta) + \gamma(\epsilon + \delta + \eta) + \delta\eta] \quad (72)$$

+ (third-order negligible terms)]

Neglecting the second-order terms, i_2 becomes

$$i_2 \simeq I h_{fe} [1 - (\gamma + \delta + \eta)]. \quad (73)$$

B. Special Low-Capacitance Sockets

Two special sockets have been designed, and are shown in detail in Figs. 16 and 17.

The socket of Fig. 16 will accommodate TO-5 and TO-18 packages as well as any other package of the same configuration. It should be mounted in a chassis with a 1.875-inch diameter hole. The capacitance between adjacent pins is less than 0.1 pf, and the capacitance from each terminal to the chassis is less than 0.3 pf.

The socket of Fig. 17 was designed to accommodate a Fairchild stud mount power package. The collector terminal is placed on the opposite side of the base terminal to minimize C'_{cb} . It makes contact with the can which is internally connected to the collector. The resultant C'_{cb} is less than 0.1 pf.